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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,483	09/28/2001	Hideaki Takahashi	ASA-1035	2770

7590 06/16/2004  
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EXAMINER

TU, CHRISTINE TRINH LE

ART UNIT PAPER NUMBER

2133

DATE MAILED: 06/16/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/964,483

Applicant(s)

TAKAHASHI ET AL.

Examiner

Christine T. Tu

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-17, 22 and 23 is/are allowed.
- 6) ☒ Claim(s) 18-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 18-21 are rejected under 35 U.S.C. 102b) as being anticipated by Tamamura et al. (5,579,236 and Tamamura hereinafter).

Claims 18, 19 and 21:

Tamamura teaches (figure 1) that within a semiconductor apparatus, a signal generating source (1) generates an analog voltage at terminal "b" and is connected to a DUT. The analog voltage at terminal "b" is also fed back to a current measuring circuit (3), then the current measuring circuit outputs a voltage measure value  $V_{MOUT}$  to be fed back into the signal generating source (1) (figure 1, column 1 lines 9-14, column 5 lines 9-column 6 line 5).

Claim 20:

Tamamura shows (figure 1) that the signal generating source (1) comprises a DAC (12) for converting a digital signal into an analog signal and such an analog signal later is outputting as  $V_{out}$ .

***Allowable Subject Matter***

2. The following is a statement of reasons for the indication of allowable subject matter:

3. The present invention pertains a semiconductor apparatus having an analog generating circuit.

The prior arts of record, however, does not teach an analog generation circuit including a resistive element, a capacitive element and switching element(s) for generating a voltage determined by a conduction time of the switching element and by a time constant of the resistive and capacitive elements based on a current flowing through the resistive element controlled by turning ON and OFF of the switching element(s), wherein the output voltage of the analog generation circuit is fed back to the analog generation circuit for generating the output voltage according to the fed-back voltage.

The prior arts of record does not teach the analog cell including variable wiring means having switching elements for connecting or disconnecting a plurality of signal lines for connection of the analog generation circuit with at least another variable logic circuit and signal lines mutually intersected, and wiring-line connection state memory means for storing states of the switching elements of the variable wiring means.

Thus claims 1-17 and 22-23 are allowable over the prior arts of record.


4. Claim 1-17 and 22-23 allowed.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Christine T. Tu  
Primary Examiner  
Art Unit 2133

June 3, 2004